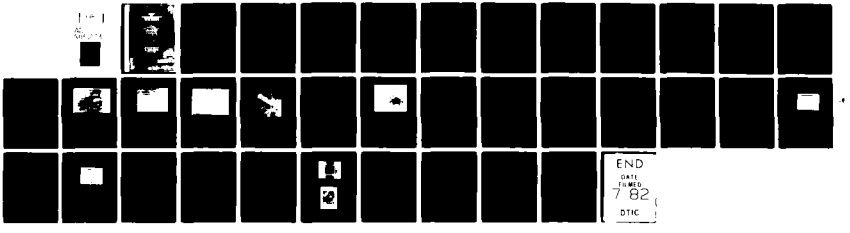
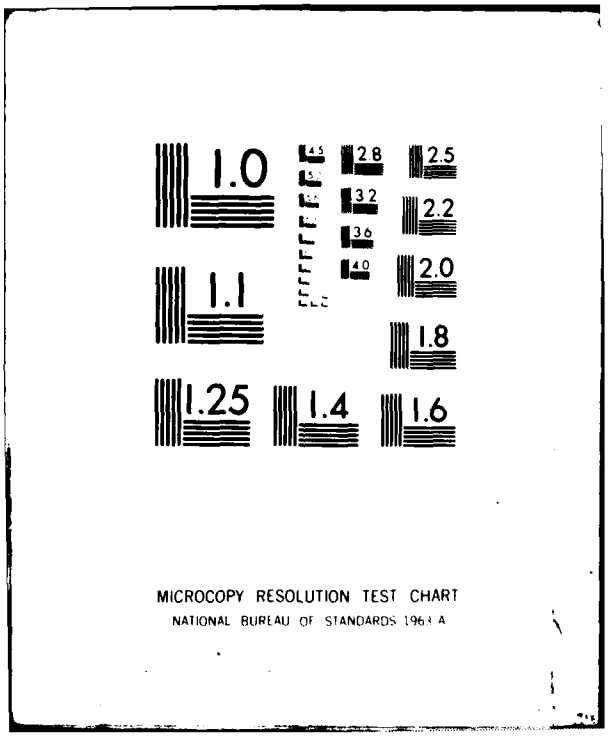
AD-A115 273 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 20/2
LATERAL SEEDING OF SILICON-ON-INSULATOR.(U)
APR 82 H W LAM, R F PINIZZOTTO N00014-81-C-0461
UNCLASSIFIED TI-08-82-17 NL

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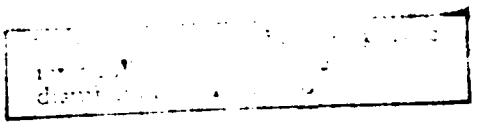
REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A115 273 / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Lateral Seeding of Silicon-on-Insulator	5. TYPE OF REPORT & PERIOD COVERED Final Report 1 July 1981 - 31 December 1981
	6. PERFORMING ORG. REPORT NUMBER 08-82-17
7. AUTHOR(s) H. W. Lam and R. F. Pinizzotto	8. CONTRACT OR GRANT NUMBER(s) N00014-81-C-0461
9. PERFORMING ORGANIZATION NAME AND ADDRESS Texas Instruments, Incorporated Central Research Laboratories 13500 N. Central Expwy., Dallas, TX 75265	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research 800 North Quincy Street Arlington, VA 22217	12. REPORT DATE April 1982
	13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report) Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)



17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Scientific Officer - Mr. M. N. Yoder

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Silicon-on-Insulator
Dielectric Isolation
Micro-zone Melting
Silicon Crystal Growth
Silicon Thin Film

Micrometer deg.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A micro-zone melting growth process using a scanning line-shaped graphite heater has been developed to produce (100) silicon-on-insulator (SOI) material over a three inch wafer. Very low angle grain boundaries (less than 0.3°) still exist extensively in the material. A 2 μm thick layer of plasma CVD oxide deposited from N_2O and SiH_4 has been found to be an effective capping structure in preventing the molten silicon from beading up. A SiC coating on the top heating element is used to prevent carbon contamination of the recrystallized film. CMOS devices have been fabricated in the recrystallized SOI

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material. Surface electron and surface hole mobility values of typically 600 cm^2/V-s and 300 cm^2/V-s, respectively, have been measured. The leakage current is uniformly low, typically in the 10^{-13} A/μm channel width range at V_{DS} = 1 V. It has also been determined that the low angle grain boundaries do not have a primary effect on the carrier mobility. Furthermore, the problem of enhanced diffusion of arsenic along the grain boundaries is significantly less severe in the present SOI material. The small protrusions found in the surface of the recrystallized film did not contribute to gate shorts in the devices measured. However, they may present a reliability problem. Attempts are underway to improve the process to eliminate the protrusions.

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SECTION I
INTRODUCTION

The goal of this program is to develop the scanned graphite strip heater recrystallization process for the growth of silicon-on-insulator (SOI) material.

SOI material with (100) orientation has been successfully grown using a scanning argon ion laser[1] and a scanning graphite strip heater.[2] The scanned graphited heater process developed thus far was for a limited area growth and the resulting material has not been fully characterized.

In this program, a process was developed for the recrystallization of a full three inch wafer and very detailed characterization of the material was pursued.

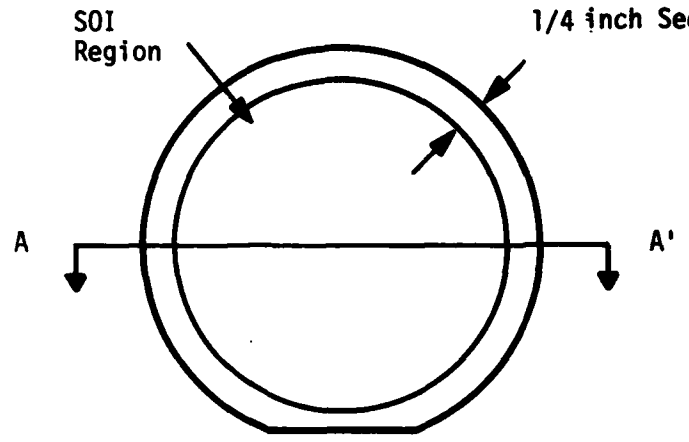
In Section II, the recrystallization process is described. Section III compares the several capping structures used. In Section IV, the physical characterization of the material, using primarily transmission electron microscopy, is described. In Section V, the problem of carbon contamination and solutions to overcome the contamination are described. Results of MOSFETs fabricated in this SOI material are reported in Section VI. A summary of the work is presented in Section VII.

Section II
THE SCANNED GRAPHITE RECRYSTALLIZATION PROCESS

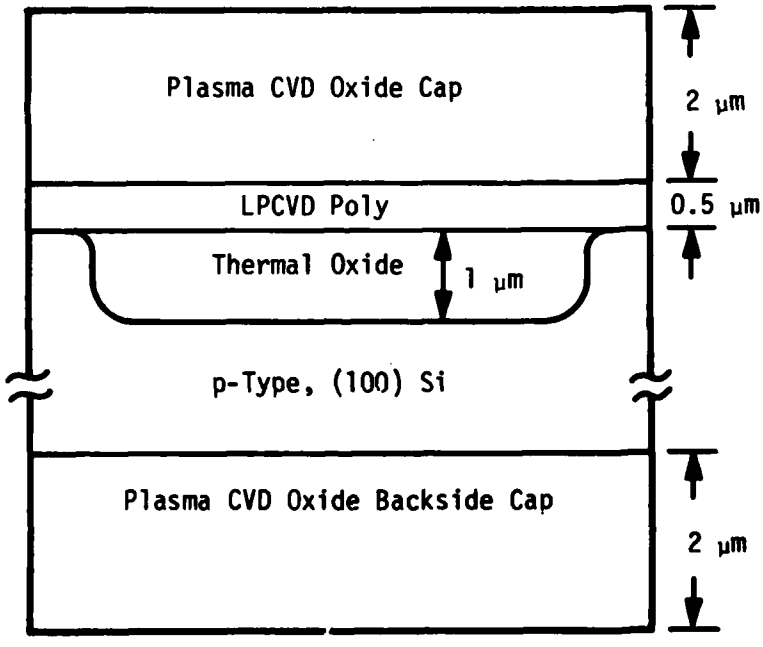
The substrates used in our experiments were (100) Czochralski grown silicon wafers. They were 76 mm in diameter, p-type, with resistivities of 6 to 8 Ω-cm. The wafers were cleaned using standard IC fabrication techniques. A 100 nm thick layer of silicon dioxide was thermally grown at 1000°C. Seeding areas for lateral epitaxial growth were photolithographically defined. A 1 μm thick fully recessed oxide layer is then grown in the center portion of the wafer. A 500 nm thick layer of polycrystalline silicon was then deposited on the wafers in a low pressure chemical vapor deposition reactor. The wafers were completely covered, front and back, with a 2 μm thick layer of silicon dioxide in a plasma chemical vapor deposition system (See Section III). The oxide cap protects the polysilicon and improves the uniformity of the recrystallization process. The resulting structure is shown in Figure 1.

Micro-zone recrystallization was done using a scanning graphite strip heater reactor similar to the one described by Fan et al.[2] (Figure 2). The wafers were processed individually. Before heating began, the strip heater reactor was vacuum pumped to a pressure of less than 6 kPa and back filled with Ar to a pressure of 125 kPa, slightly above atmospheric pressure. The bottom stationary graphite heater was used to raise the surface temperature of the wafer to 1200°C, as measured with a pyrometer. The movable top graphite strip was heated to 2000°C. It was scanned across the surface of the wafer at a constant speed of 2 mm/s using a motor driven system.

The polycrystalline silicon layer melts by absorption of radiant heat from the top graphite strip heater. When the heat source is moved far enough away, the molten silicon cools and recrystallizes. If the liquid silicon is in contact with the substrate, it recrystallizes epitaxially. The newly formed single crystal areas act as seeds for the crystal growth of the silicon



(a) Top View



(b) Section View AA'

Figure 1 Configuration of Wafer for Scanned Graphite Heater Recrystallization

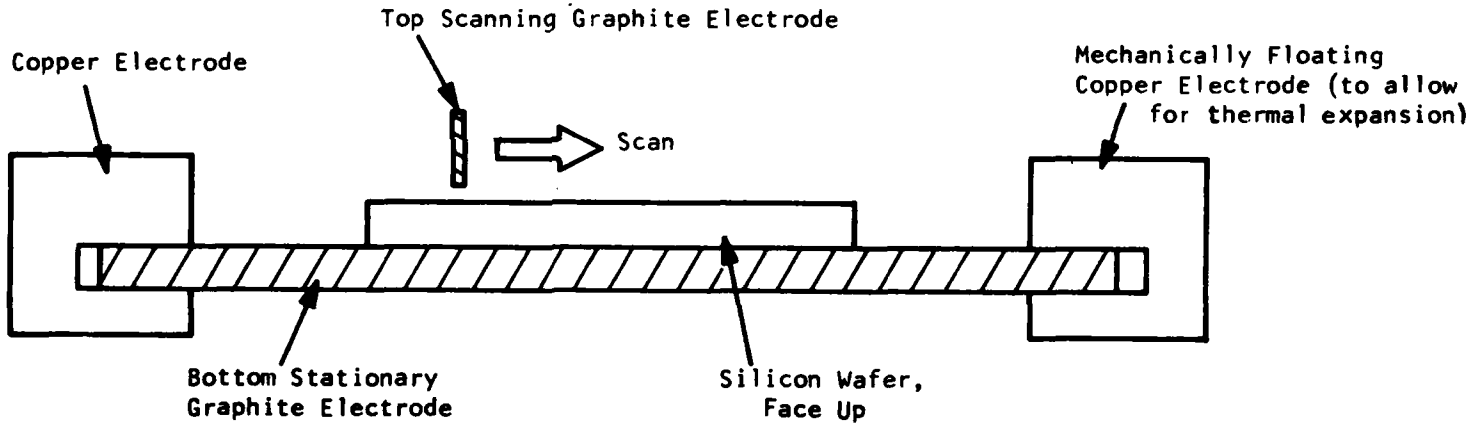


Figure 2 Schematic of The Scanned Graphite Strip Heater Equipment.

on top of the silicon dioxide layer. The epitaxial seeds form first because the removal of heat through the silicon substrate is much faster than heat transfer through the oxide.

The two most crucial parameters in the recrystallization process are the distance between the top heating element and the silicon wafer, and the uniformity of the temperature profile of the silicon wafer.

When the bottom heating element (Figure 2) is heated from room temperature to the operating temperature of 1200°C, the bottom heating element will expand. Therefore, one of the electrodes is left mechanically floating to absorb the expansion. This is crucial in maintaining a constant gap between the top heating element and the wafer.

The temperature profile of the bottom heating element (and therefore the wafer) can be tailored by altering the geometrical shape of the bottom element. By a trial and error process, a very uniform profile can be obtained.

It was determined that the variation across a three inch wafer should be less than ± 5°C. Otherwise it will result in a nonuniform melting across the wafer. With proper tailoring, a ± 2°C maximum variation has been obtained.

This resulted in a recrystallization process that is uniform across a full three inch wafer. The next improvement will be to tailor the temperature profile of the top heating element.

SECTION III
THE CAPPING STRUCTURE

Several different capping structures were experimented with: 2 μm thick layer of APCVD oxide; 2 μm thick layer of plasma CVD oxide deposited from CO_2 and SiH_4; 2 μm thick layer of plasma CVD oxide deposited from N_2O and SiH_4; and a 30 nm thick layer of sputtered silicon nitride layer on the various oxide capping layers.

A proper capping structure allows the molten silicon to wet the cap and underlying insulator surfaces and prevents the molten silicon from beading up. Furthermore, it helps to prevent impurities from diffusing into the silicon film.

It was found that the APCVD oxide cap was unsatisfactory as it tends to crack at elevated temperatures. Furthermore, the molten silicon has a high tendency to bead up. It was also found that the deposition of a 30 nm thick layer of sputter-deposition silicon nitride improves the film adhesion, but the results are unsatisfactory.

It was found that the plasma CVD oxide film deposited from CO_2 and silane gives satisfactory results as the recrystallized layer remains smooth and continuous. However, because of carbon contamination introduced by this oxide cap (Section V), this capping structure was also found to be unsatisfactory.

The plasma CVD oxide cap deposited from N_2O and silane was found to be the best choice. The index of refraction of this oxide film is typically 1.47 to 1.48, higher than that of thermal oxide (1.45). It is believed that this

CVD process tends to incorporate nitrogen into the oxide film, thereby increasing the index of refraction. This capping structure results in a smooth recrystallized film and no carbon contamination is introduced by this cap structure. It was found that with the use of the plasma CVD oxide cap (N_2O, SiH_4), the sputtered nitride layer is no longer necessary to obtain a satisfactory recrystallization result.

SECTION IV
PHYSICAL CHARACTERIZATION OF THE RECRYSTALLIZED SOI MATERIAL

Figure 3 is a Nomarski contrast optical micrograph of part of a wafer that was strip heater recrystallized. The sample was Secco etched[3] to reveal the microstructural defects in the material. The interference fringes are the result of variations in the thickness of the top silicon layer. The darker rectangular areas, such as the one indicated by an α in Figure 3, are the seed areas where the polycrystalline silicon film was in direct contact with the silicon substrate. The strip heater was scanned diagonally across the pattern from the upper left hand corner to the lower right corner. The long, linear defects, for example the one labeled β in Figure 3, are low angle grain boundaries. Figure 4 is a higher magnification view of the lower right hand corner of Figure 3, similarly labeled, which shows the defects in more detail. These defects are classified as sub-grain boundaries and not as true grain boundaries because they are composed of discrete dislocations and are not abrupt planar changes of crystal orientation. The boundaries are formed by dislocation coalesence and can be described by combinations of regular dislocation arrays. Figure 5 is a weak beam g(3 g) TEM micrograph of one such sub-grain boundary. The individual dislocations of two arrays are clearly discernable. In a true, large angle grain boundary, the misorientation of the grains cannot be described by dislocation networks and the boundary appears to be an abrupt planar defect with defect free crystals on both sides. Figure 6 is a lower magnification TEM micrograph of a low angle grain boundary that also shows the interior of the grains on either side of it. No defects are detectable within the grains. The recrystallized material between the sub-grain boundaries is defect free.

Figure 3 Nomarski Contrast Optical Micrograph of Part of a Silicon Slice that was Scanning Graphite Strip Heater Annealed. It has been Seeco etched to reveal microstructural defects.

Figure 4 A Higher Magnification View of the Lower Right Hand Corner of Figure 3

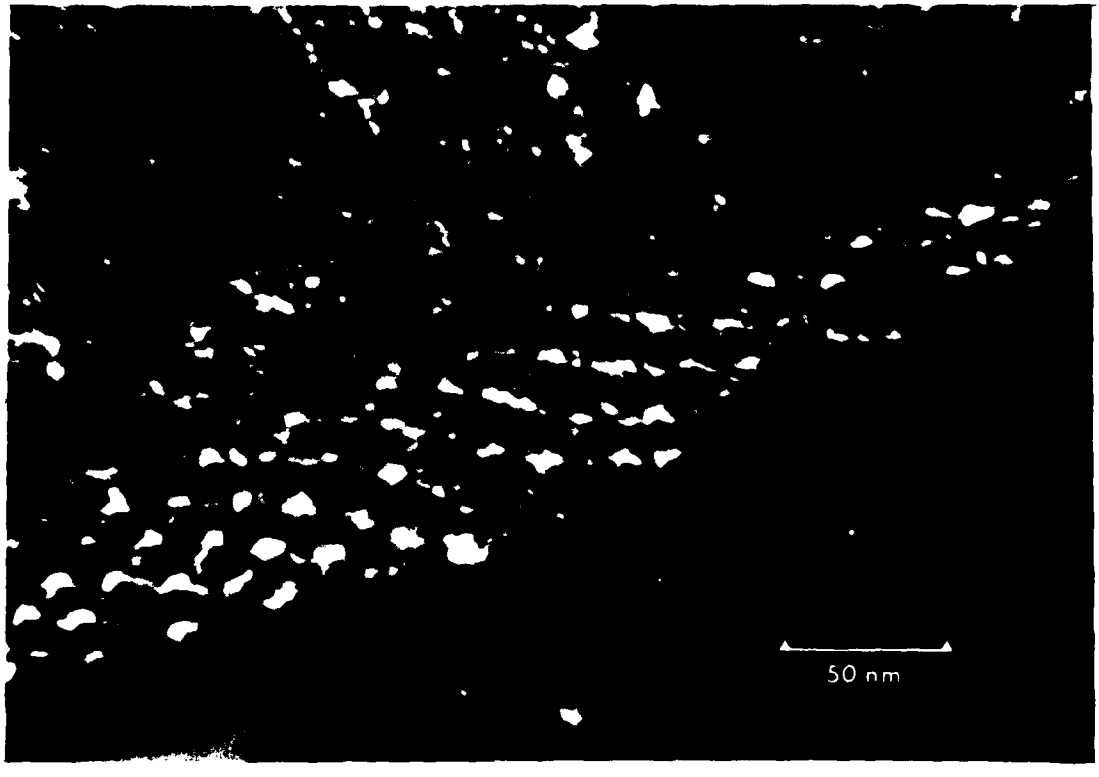


Figure 5 Weak Beam g(3 g) Transmission Electron Micrograph of a Low-Angle Grain Boundary. Two sets of dislocations are clearly visible.

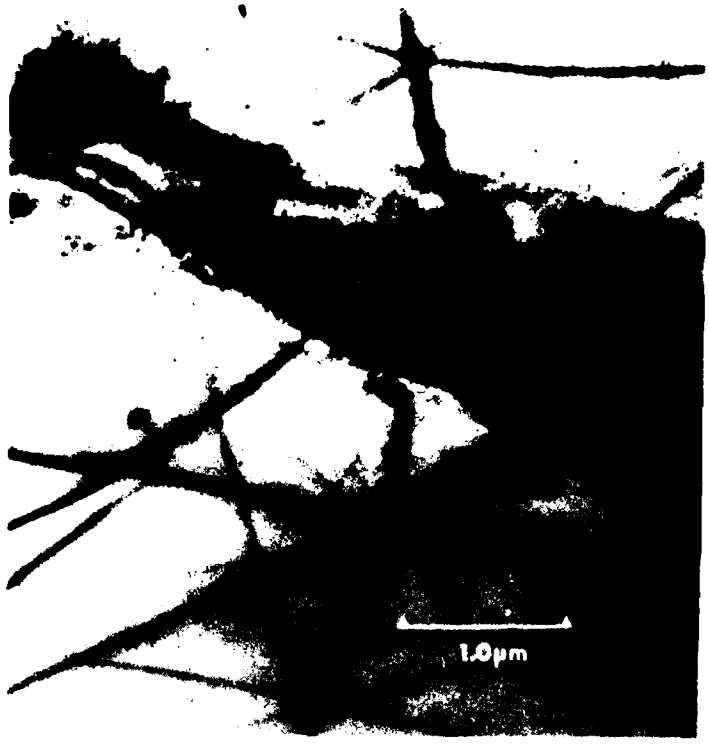


Figure 6 Bright Field Transmission Electron Micrograph of a Low-Angle Grain Boundary. There are no internal defects in either grain. The dark particles are β-SiC.

The average distance between sub-grain boundaries is much larger for graphite strip heater recrystallized material than for laser annealed material. There are at least two possible explanations for this observation, both based on our proposal,[4] that the dislocations in laterally seeded SOI are generated by the stresses which arise from the increase in the volume of solid silicon compared to liquid silicon. First, slower growth rates will improve the quality of the recrystallized films because less trapping of liquid by surrounding solid will occur. The results obtained for graphite strip heater recrystallization support this prediction. In the strip heater case, scan speeds of 1 to 2 mm/s are used and the average grain size is on the order of millimeters. In laser recrystallization, scan speeds of 100 to 150 mm/s are common and the grain size is typically 50 μm. Second, the beam size in the two cases is quite different. The larger melt zones formed when using strip heaters, compared to lasers, will lead to an increase in grain size. This is a result of the formation of smoother growth fronts caused by the larger radius of curvature of the molten zone.

The RHEED pattern, including the area shown in Figure 3, is presented in Figure 7. The top silicon layer is (100) in orientation and is of high crystalline perfection as evidenced by the clarity of the Kikuchi lines in the pattern. Our RHEED apparatus samples an area about 0.1 mm by 10 mm, hence the pattern shown was obtained from an area several times larger than that shown in Figure 3. There is no evidence of polycrystalline silicon or of any significant variance of orientation in the top layer. However, diffraction rings resulting from the presence of β-SiC are clearly defined. ESCA was used to monitor the carbon levels in our samples before and after recrystallization in the graphite strip heater reactor. In all cases, 40 nm of material were removed by Ar ion sputtering immediately before ESCA. This minimizes surface adsorption effects and uncovers bulk material for analysis. Before recrystallization, C was not detected in the silicon substrate, the polycrystalline silicon or in the plasma oxide capping layer. After recrystallization, C was found in both the oxide cap and in the recrystallized top silicon layer. The

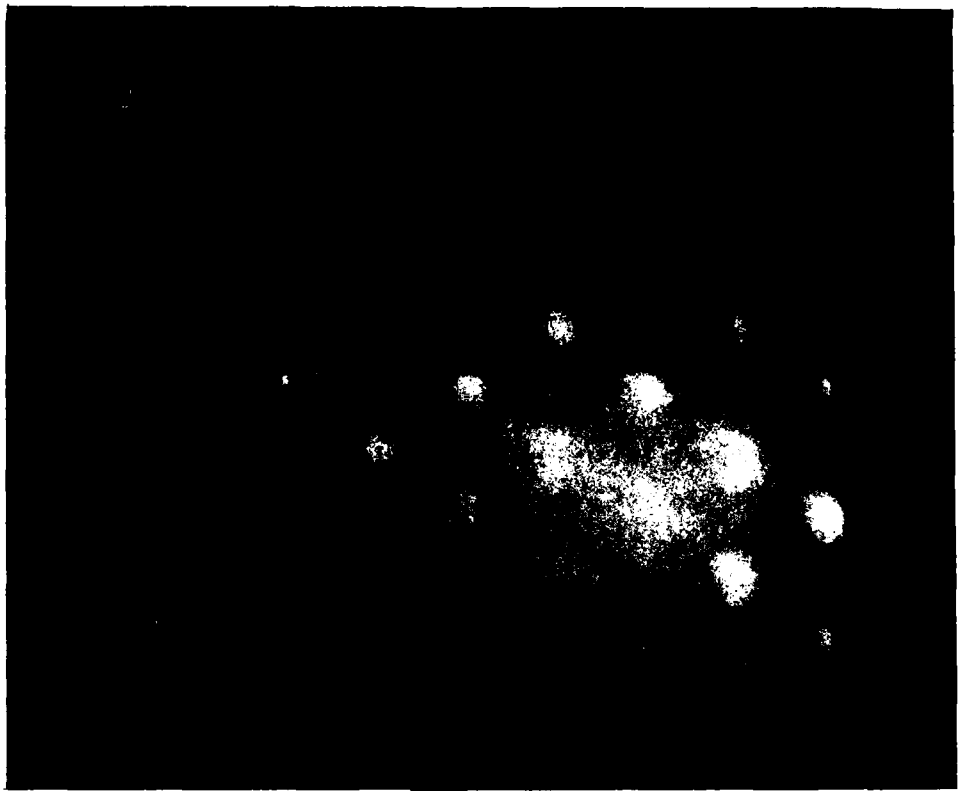


Figure 7 A RHEED Pattern Showing that the Top Silicon Layer is Single Crystal, but Contains β-SiC.

energy of the ESCA peak corresponds to carbide formation in both cases. Absolute SiC concentrations are not known because we do not have standard samples of SiC in either silicon dioxide or in silicon for calibration. We believe that the carbon contamination was caused by small particles of graphite falling from the top heater onto the slices. Some of the larger particles could be observed with an optical microscope. Modifications are being made that are expected to alleviate this problem. While it is possible that gas phase transport of C may occur, it is certainly an unimportant effect compared to direct particulate contamination.

Electron channeling patterns were used to investigate the degree of misorientation across the sub-grain boundaries shown in Figures 3 and 4. In our instrument, a JEOL 100 CX with a field emission electron gun, the patterns are obtained from areas approximately 5 μm in diameter and have a resolution better than 0.1°. Backscattered electrons were used to form the images in order to enhance the contrast. In all cases, the change in orientation, either by rotation in the plane of the top silicon layer or by tilt out of the plane, was less than 0.3°. Usually it was less than 0.2°. This is consistent with the TEM results since such small misorientations are easily accomodated by dislocation arrays. While it may be possible to classify this material as single crystal, the number and types of defects observed demonstrate that it is not yet of the same high quality as either Czochralski or float-zone silicon.

SECTION V
SOLUTIONS FOR THE CARBON CONTAMINATION PROBLEM

Sputtered Auger electron spectroscopy was used to study the carbon contamination in the recrystallized silicon film after the removal of the 2 μm silicon dioxide cap. Figure 8 shows the spectrum of a polysilicon film before the recrystallization. The atomic percentage measurement should be used only as a relative measure as we cannot calibrate the measurement against a standard. Furthermore, hydrocarbon is always present as a result of the oil used in the vacuum pumps. The horizontal axis is the sputtering time in minutes. Approximately 4 nm of silicon are sputtered per minute so that the sputter time axis is equivalent to a depth axis.

Figure 9 shows the sputtered Auger electron spectrum of a recrystallized silicon layer. This layer was capped with a 2 μm thick APCVD oxide layer and the top heating element was made of POCO DFP-3-2 material (with specific gravity of 1.88). The carbon content of this silicon film is very high. Apparently, when the top heating element is thermally stressed, small particles of carbon drop from the top heating element, diffuse rapidly through the cap and dissolve into the molten silicon. Other possible sources of carbon contamination are: the bottom stationary heating element, back-streaming of oil from the mechanical pump, and the oxide cap layer that is deposited from a plasma CVD process using CO_2 gas and SiH_4 gas. Of the four possible sources, the top heating element and the oxide cap layer are the most likely contributors to the contamination because they are the members that are most severely temperature-stressed.

To prove that hypothesis, a graphite heater was coated with a silicon carbide coating. Some wafers were recrystallized with the coated top heating element and the carbon concentration was measured. The result of that measurement indicated that the carbon contamination was reduced to about 7 or 8 percent, substantially smaller than the 30 percent observed earlier.

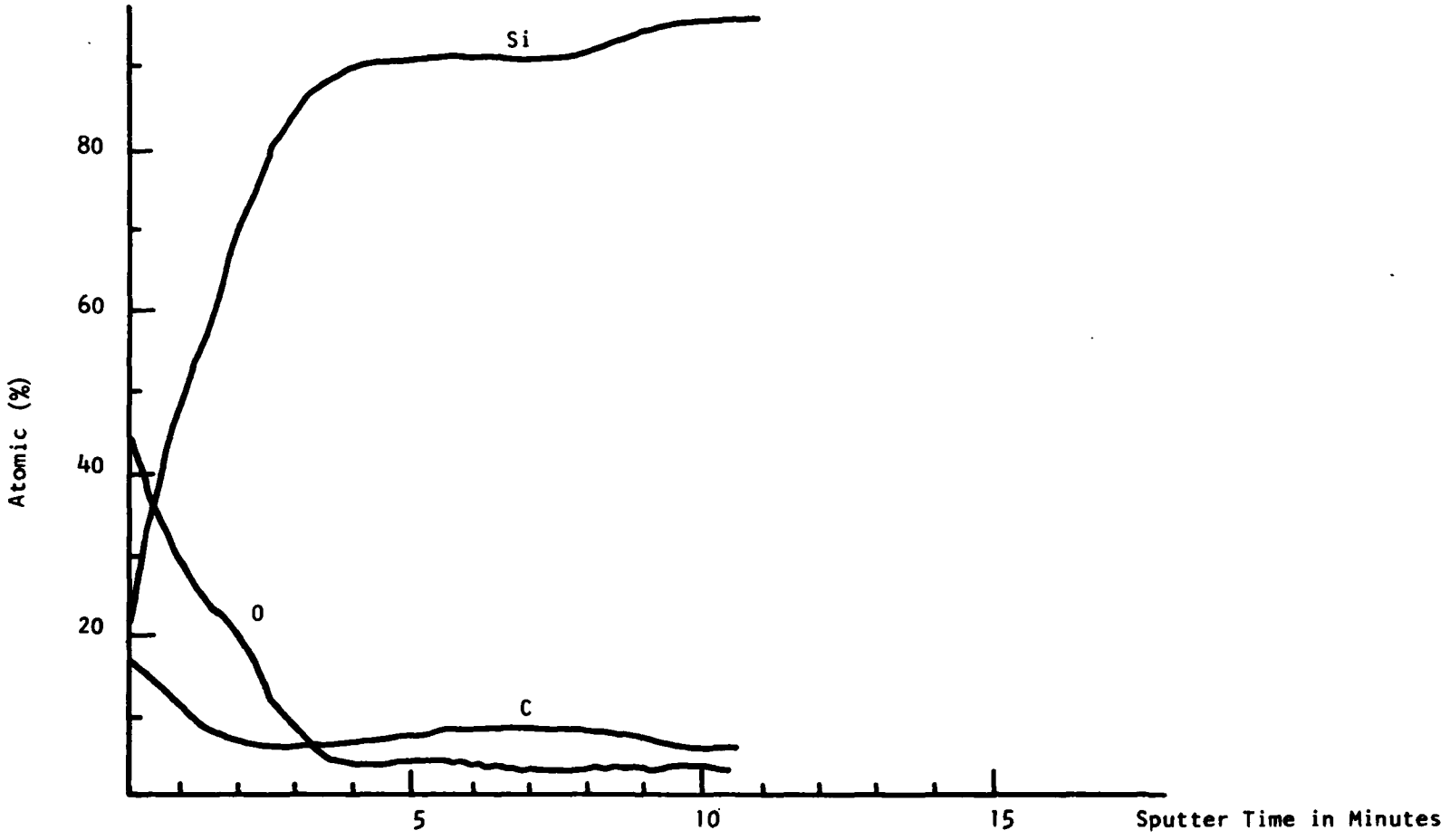


Figure 8 Sputtered Auger Electron Spectrum of Polysilicon Before Recrystallization. Horizontal axis: 1 minute = 4 nm

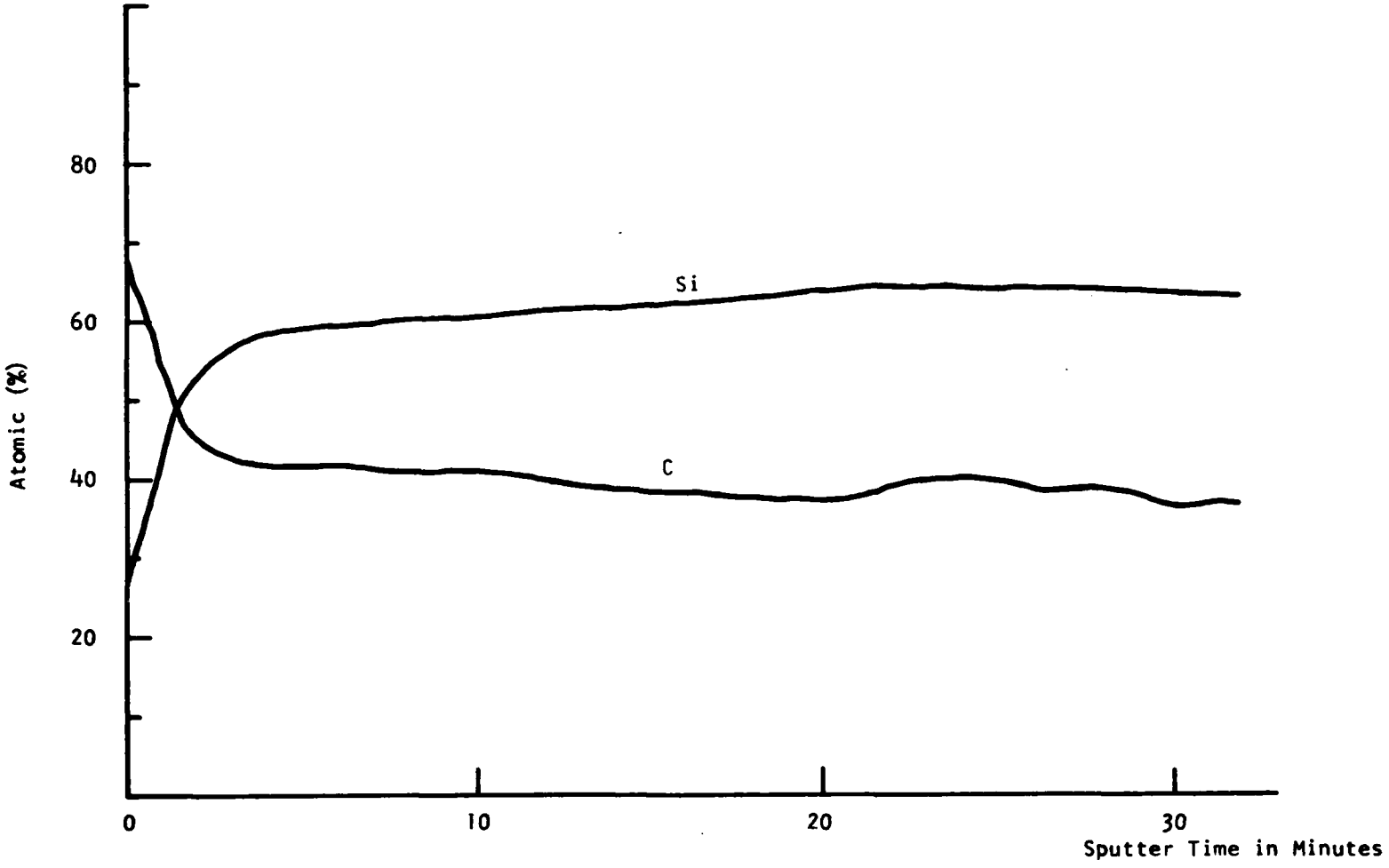


Figure 9 Sputtered Auger Electron Spectrum of Recrystallized Silicon With a 2 μm APCVD Oxide Cap.

Because the CVD oxide cap is deposited from CO_2 and SiH_4 gas sources, carbon is present in the oxide cap. Furthermore, the cap is in contact with the silicon so that when the silicon melts, dissolution of the carbon into silicon is highly possible. Therefore, a plasma CVD oxide cap deposited from N_2O and SiH_4 gas sources was developed. This oxide layer has an index of refraction of 1.47 to 1.48, slightly higher than that of thermal oxide, which is 1.45. It is believed that this oxide layer contains nitrogen, which is responsible for a higher index. After a silicon wafer capped with this new oxide layer is recrystallized with a silicon carbide coated strip heater, the carbon contamination in the bulk is reduced to about 3 percent, the noise level of the measurement technique. There is a layer of about 10 to 15 nm at the surface where the carbon concentration is still high. However, once that layer is removed the remaining silicon is free of carbon contamination. It is presently not understood why the top surface is contaminated while the bulk is not contaminated.

Additionally, attempts were made to investigate the feasibility of using other monolithic or coated graphite material as the top heating element. Besides the POCO DFP-3-2 material, Ultra Carbon UT44 material, (with a specific density of 1.80) and Ultra Carbon pyrolytically coated material have also been used. The carbon contamination problem existed in the silicon layer recrystallized by these material. Therefore, the silicon carbide coated graphite is the only material that proved satisfactory.

One constraint to the use of a silicon carbide coated material is that the coating will oxidize in oxygen at an elevated temperature to $SiC + O_2 \rightarrow SiO + CO$. If the reaction chamber is not air tight, the coating will be consumed.

Furthermore, silicon carbide sublimes. The sublimation temperature is about 1900°C. Therefore, the temperature of a silicon carbide coated top heating element should be held substantially below 1900°C.

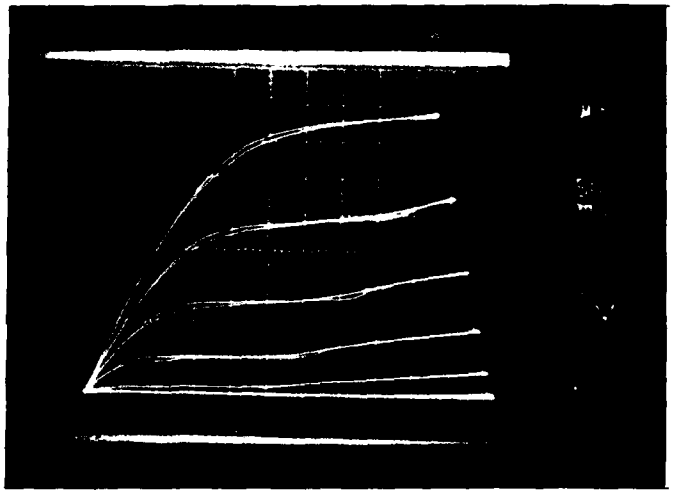
SECTION VI

MOSFET DEVICE FABRICATION AND CHARACTERIZATION

After the recrystallization process, the 2 μm oxide cap is removed by etching in a buffered HF solution. Because the top 10 to 15 nm silicon surface layer is known to contain carbon contamination (See Section V) it is removed by oxidation in steam at 900°C, followed by an etch in buffered HF solution. Subsequently, the wafers are processed with a CMOS process using complete-island-etch as the device to device isolation. The gate oxide thickness was 60 nm.

Some typical device results are shown in Figures 10 to 13. Figure 10 shows the drain current of a 25 μm/5 μm (W/L) n-channel device as a function of drain bias with different gate voltages. The kinks in the I-V characteristics are clearly evident. The surface electron mobility is calculated to be 621 $cm^2/V\text{-}s$, comparable to that of bulk-type devices. The threshold voltage is about 1 V more positive than expected. This positive shift is also observed in the p-channel devices. Subsequent investigation points to a p-type impurity in the as deposited polysilicon. A clean-up of the LPCVD deposition system eliminated the impurity in the as deposited film. Figure 11 shows the subthreshold characterization of the same device shown in Figure 10. Minimum leakage current is about 0 to 1 pA/ μm channel width at V_{DS} = 1 V. This result is substantially better than that of the laser-annealed SOI and SOS results. This is attributed to the very low defect density in this material.

Figure 12 shows the I-V characteristics of a typical p-channel device. The surface hole mobility is 302 $cm^2/V\text{-}s$, again comparable to bulk type devices. Figure 13 shows the subthreshold characteristics of the same device shown in



n-Channel 6662-20
W/L = 25 μm/5 μm
T_{ox} = 70 nm
μe = 621 cm^2/V-s in Linear Region

Figure 10 I-V Characteristics of n-Channel MOSFET

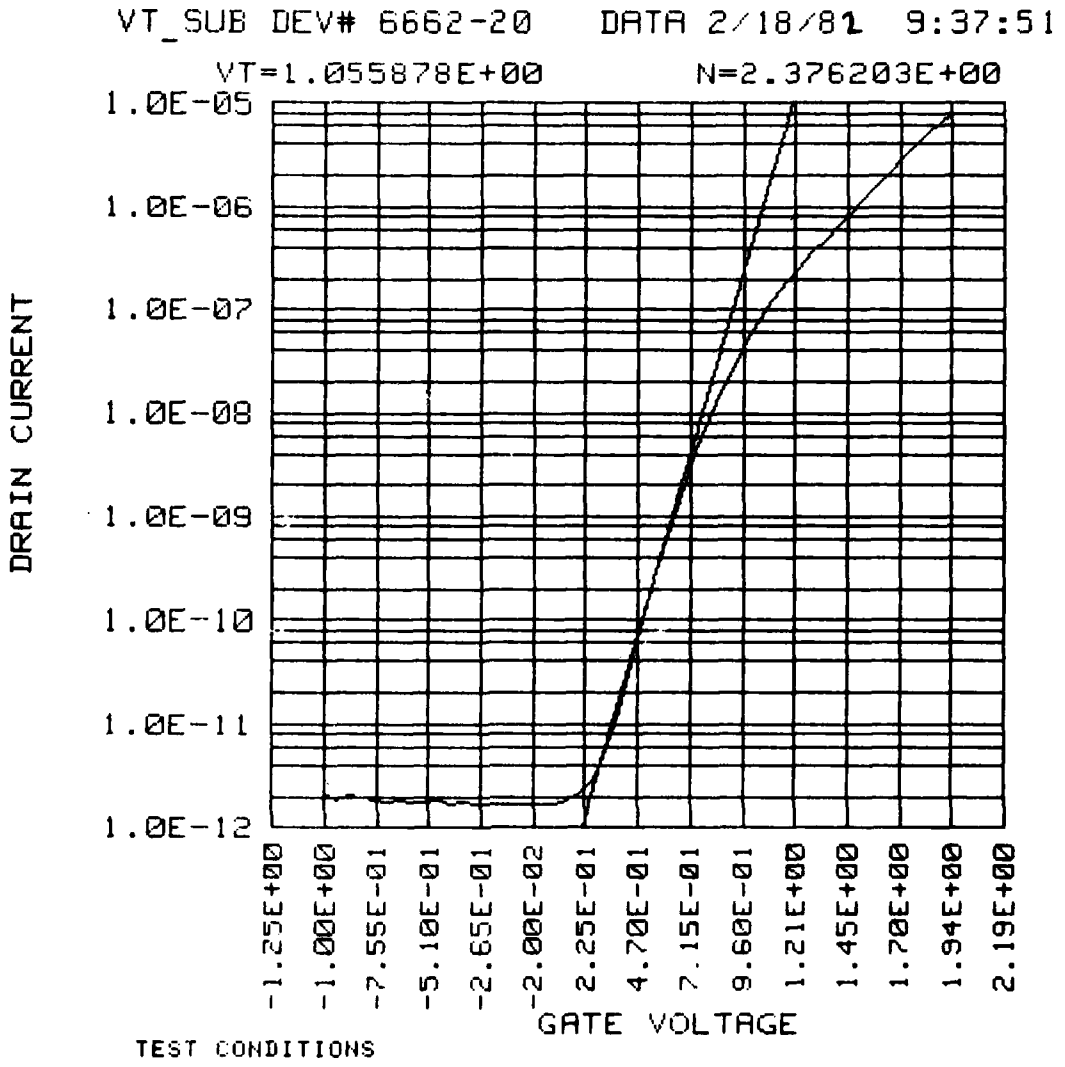
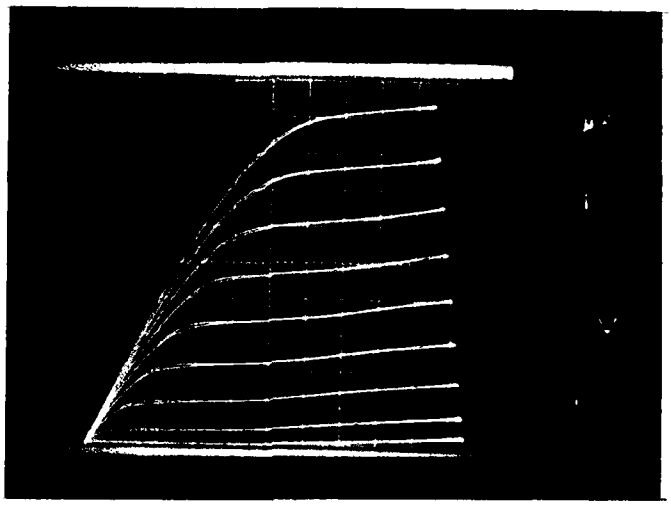


Figure 11 Subthreshold Characteristics of the n-Channel Device Shown in Figure 10



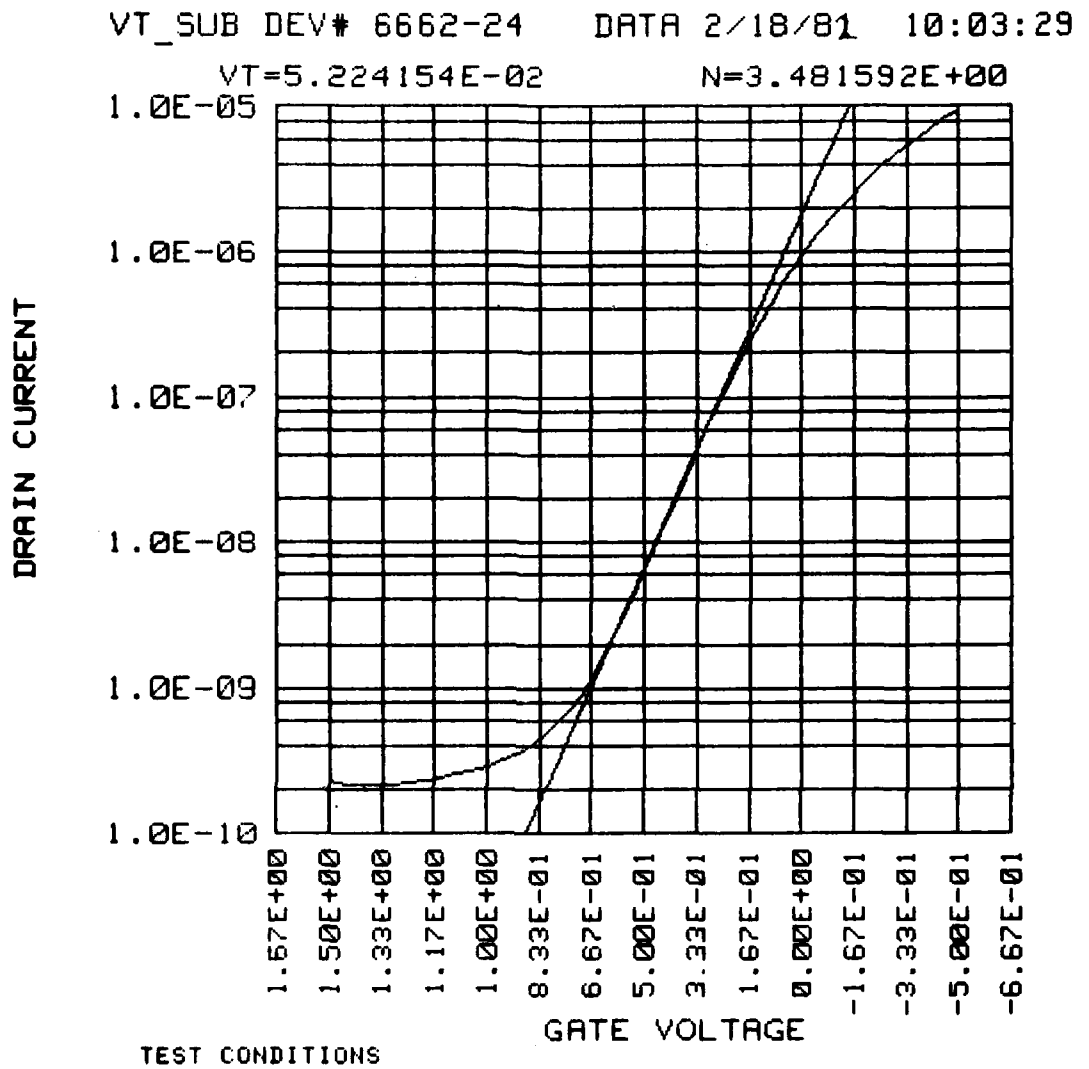
p-Channel 6662-24

W/L = 25 μm/5 μm

T_{ox} = 70 nm

μe = 302 cm^2/V-s in Linear Region

Figure 12 I-V Characteristics of a p-Channel Device



TEST CONDITIONS

P CHANNEL DEVICE

W/L= 25 / 5 Tox= 700

GATE SCAN VOLTAGES FROM 1.5 TO -1
DRAIN VOLTAGE= -1
SUBSTRATE BIAS= 0

Figure 13 The Subthreshold Characteristics of the n-Channel Device Shown in Figure 12

Figure 12. Because of the p-type impurity in the starting film mentioned above, a buried channel device resulted. The buried channel probably leads to the inability to completely shut off the drain current in the subthreshold region.

The leakage current in all the n-channel devices was measured. It was found that the leakage current is, without exception, in the 10^{-13} A/μm channel width region at V_{DS} = 1 V. The uniformity of the low leakage current is very encouraging. Furthermore, by knowing the doping concentration, the oxide thickness of the underlying oxide layer, and the back bias required to turn on the back channel, the oxide charge density at the back interface is estimated to be 5×10^{11} cm^{-2}. This is low enough to allow a design of a simple CMOS process.

After the electrical characterization was completed, the wafers were etched in a Secco solution to reveal the grain structure in the channel region. The electrical characteristics and the microstructural characteristics were then compared carefully for each device. It was found that:

1. The mobility of the device depends on the extent of the melting. If the melting is not extensive, the mobility is lower and Secco etch reveals a higher etch pit density (dislocation density). The etch pit density is inversely proportional to the mobility while the low-angle grain-boundaries only affect the mobility in the second-order fashion. For example, for a device that contains a high etch pit density, and no low-angle grain-boundaries, the mobility is lower when compared to a device with a relatively lower etch pit density and the existence of one or two low-angle grain-boundaries. It should be noted that the etch pit density is a function of the state of melt that the silicon experienced, which is controllable by the temperature of the heaters. For devices fabricated in regions that were extensively melted (where the etch pit density is low) the

mobility is high (~ 620 $cm^2/V\text{-}s$) and uniform (± 5%). We can conclude that the uniformity is significantly better than that of the laser case, that the value of the mobility is significantly higher, and that the low-angle grain-boundaries have only a second-order effect on the mobility.

2. The problem of enhanced arsenic diffusion is significantly less in the case of the scanned graphite material and cannot be detected with the method we used. Figures 14 and 15 show the active channel region of a MOSFET fabricated in the scanned graphite recrystallized material and in the laser-annealed material, respectively. Because the source-drain regions were heavily doped, they were removed much faster than the undoped channel region. The grain-boundaries and the defect regions have a higher etch rate and therefore show up in the unetched channel region. In the laser-anneal case (Figure 15) it can be seen that some notches have been etched at the location where grain-boundaries propagate from the source (or drain) region to the channel region. Because of an enhanced diffusion of arsenic along the grain-boundaries, an accumulation of arsenic at the grain-boundaries immediately adjacent to the source (or drain) area results. This led to an increased etch rate of the grain-boundary area by the Secco etch, resulting in the formation of these notches. These notches have not been observed in any of the scanned graphite devices. These two devices went through a similar thermal treatment (30 minutes at 1000°C) after a similar arsenic ion implantation of 1×10^{16} cm^{-2}. Therefore, it is believed that the low-angle grain-boundaries found in the scanned graphite material are less susceptible to enhanced arsenic diffusion than the laser-annealed case. Furthermore, it should be noted that the density of grain-boundaries in the scanned graphite case is significantly less than that of the laser case.

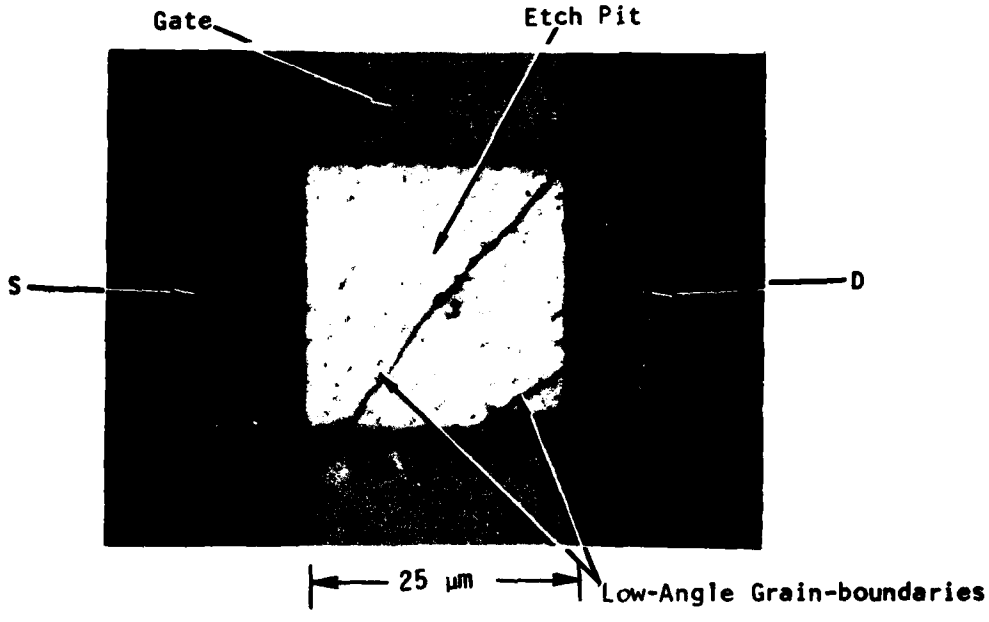


Figure 14 Channel Region of MOSFET On Scanned Graphite Recrystallized SOI

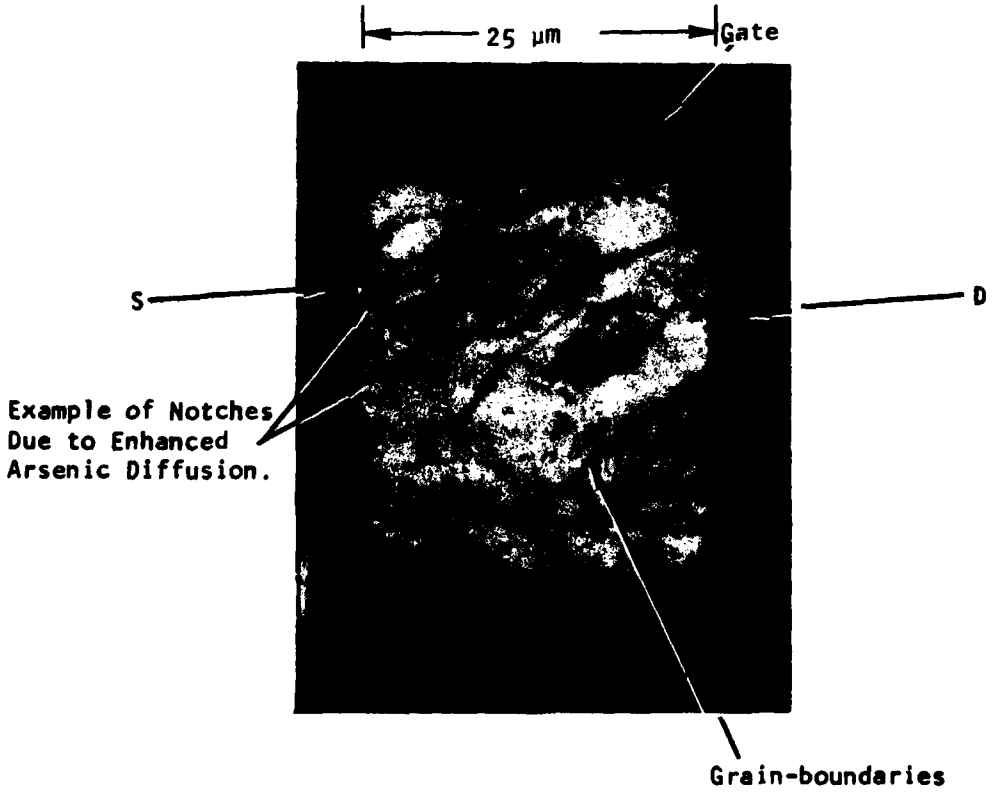


Figure 15 Channel Region of MOSFET on Laser-Annealed SOI

3. Only one device was found to have a gate short. Secco etch revealed that the shorted device does not contain one of those small protrusion regions sometimes found in the scanned graphite material. Those devices that contain one of those small protrusion regions did not show a gate short and they behave as a normal device.

SECTION VII
SUMMARY

A process has been developed where a scanning line-shaped graphite heater is used to melt and recrystallize SOI material. The process is capable of producing (100) SOI material over a three inch wafer. Very low-angle grain-boundaries (less than 0.3°) still exist extensively in the material.

It was found that a 2 μm thick layer of oxide cap produced by plasma assisted CVD deposition from N_2O and SiH_4 can properly stablize the molten silicon, preventing the molten silicon from beading up.

The low-angle grain-boundaries are probably formed when the solidification front cannot track the notion of the graphite heater. Consequently, the molten silicon is supercooled and dendrite growth from the solid propagates into the melt, resulting in the low-angle grain-boundaries between the dendrites.

A high concentration of carbon was found in the recrystallized silicon when uncapped graphite heaters were used. It is believed that small carbon particles dropped for the graphite heater when it was stressed. By capping the graphite heater with a SiC coating, the carbon contamination is eliminated. Carbon, in the form of β-SiC can only be found in a thin 10 to 15 nm layer of silicon at the surface. Otherwise, the recrystallized silicon layer is free of contamination.

CMOS devices have been fabricated in the recrystallized SOI material. Surface electron and surface hole mobility values of 600 and 300 $cm^2/V\text{-}s$, respectively, have been measured. The leakage current of the devices is uniformly low, typically in the 10^{-13} A/μm channel width range at V_{DS} = 1 V.

By comparing the grain structure revealed by a Secco etch and the electrical characteristics of the devices, it was determined that the low-angle grain-boundaries have a second order effect on the magnitude of the mobility. Furthermore, the problem of enhanced diffusion of arsenic along the grain-boundaries is less severe in the scanned graphite heater recrystallized SOI material.

It was also observed that the small protrusions at the surface of the graphite heater recrystallized SOI material did not contribute to gate shorts in the devices measured. However, they may present a reliability problem. Attempts are underway to improve the recrystallization process to eliminate the protrusions, which are believed to be caused by pockets of liquid trapped behind by the fast growing dendrites.

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